Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer, the fin having a width ranging from about 50 Å to about 200 Å and thickness ranging from 600 Å to about 800 Å in a channel region of the semiconductor device;

a source region formed on the insulating layer adjacent a first side of the fin; and

a drain region formed on the insulating layer adjacent a second side of the fin opposite the first side, wherein the source and drain regions have a greater thickness than the fin and the thickness of the source and drain regions ranges from about 700 Å to 900 Å.

2-4. (canceled)

5. (currently amended) The semiconductor device 1, further comprising:

a gate formed over a top surface of the fin in ~~a~~ the channel region of the semiconductor device.

6. (original) The semiconductor device of claim 5, wherein the gate comprises a first gate disposed on a third side of the fin and a second gate disposed on a fourth side of the fin opposite the third side.

7. (original) The semiconductor device of claim 1, further comprising:

at least one dielectric layer formed over a top surface of the fin.

8. (original) The semiconductor device of claim 7, further comprising:

a gate formed over the at least one dielectric layer and being disposed on a third and fourth side of the fin.

9. (currently amended) The semiconductor device of claim 1, wherein the insulating ~~later~~ layer comprises a buried oxide layer and the fin comprises at least one of silicon and germanium.

10-14. (canceled)

15. (currently amended) A semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end and a second end, wherein the conductive fin has a thickness ranging from about 600 Å to about 800 Å and a width ranging from about 50 Å to about 200 Å in a channel region of the semiconductor device;

a source region formed adjacent the first end of the conductive fin, the source region having a thickness ranging from about 700 Å to about 900Å; and

a drain region formed adjacent the second end of the conductive fin, the drain region

having a thickness ranging from about 700 Å to about 900Å, and wherein the source and drain regions have a greater thickness than the conductive fin in ~~a~~ the channel region of the semiconductor device.

16. (original) The semiconductor device of claim 15, further comprising:

a gate dielectric layer formed on the conductive fin in the channel region of the semiconductor device; and

a gate formed over the gate dielectric layer.

17. (original) The semiconductor device of claim 16, wherein the gate comprises a first gate electrode disposed on a first side of the conductive fin and a second gate electrode disposed on a second side of the conductive fin opposite the first side.

18. (canceled)

19. (canceled)

20. (original) The semiconductor device of claim 15, wherein the source and drain regions are each at least about 200 Å thicker than the conductive fin in the channel region of the semiconductor device.

21. (new) The semiconductor device of claim 5, wherein the gate has a thickness ranging from about 300 Å to about 800 Å.

22. (new) The semiconductor device of claim 7, wherein the at least one dielectric layer formed over a top surface of the fin comprises:

an oxide layer and a nitride layer formed on the oxide layer.

23. (new) The semiconductor device of claim 7, wherein the at least one dielectric layer formed over a top surface of the fin has a thickness ranging from about 10 Å to about 20 Å.

24. (new) The semiconductor device of claim 16, wherein the gate has a thickness ranging from about 300 Å to about 800 Å.

25. (new) The semiconductor device of claim 16, wherein the gate dielectric layer comprises:

an oxide layer and a nitride layer formed on the oxide layer.

26. (new) The semiconductor device of claim 16, wherein the gate dielectric layer has a thickness ranging from about 10 Å to about 20 Å.